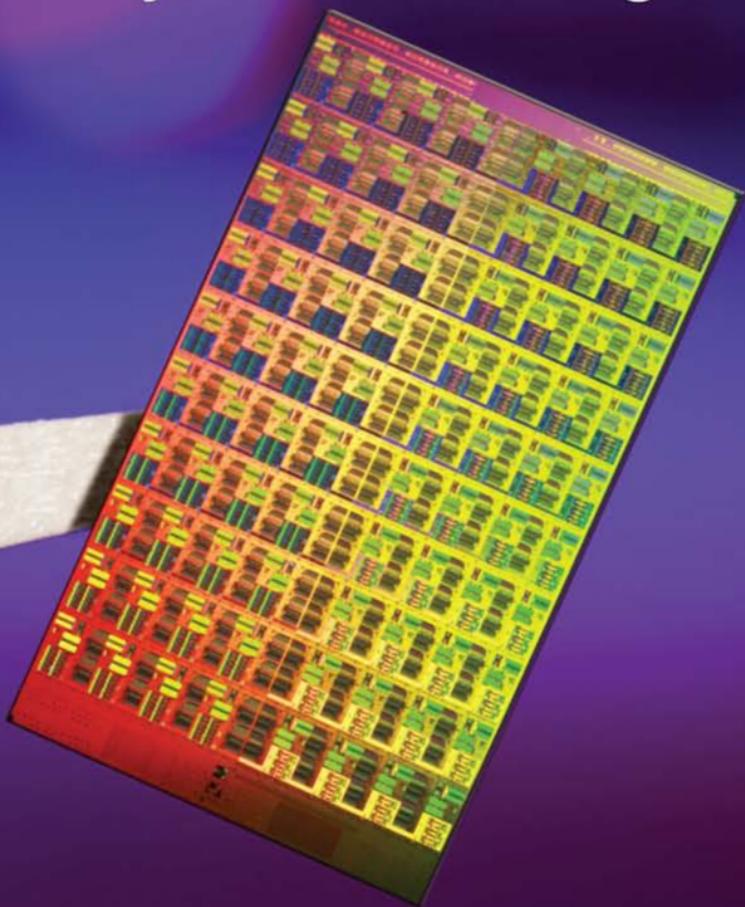


SECOND EDITION

# Digital Integrated CIRCUITS

Analysis and Design



**John E. Ayers**



CRC Press  
Taylor & Francis Group

---

S E C O N D   E D I T I O N

---

# Digital Integrated **CIRCUITS**

---

Analysis and Design



S E C O N D   E D I T I O N

---

# Digital Integrated CIRCUITS

---

Analysis and Design

**John E. Ayers**



CRC Press

Taylor & Francis Group

Boca Raton London New York

---

CRC Press is an imprint of the  
Taylor & Francis Group, an **Informa** business

CRC Press  
Taylor & Francis Group  
6000 Broken Sound Parkway NW, Suite 300  
Boca Raton, FL 33487-2742

© 2010 by Taylor & Francis Group, LLC  
CRC Press is an imprint of Taylor & Francis Group, an Informa business

No claim to original U.S. Government works  
Printed in the United States of America on acid-free paper  
10 9 8 7 6 5 4 3 2 1

International Standard Book Number-13: 978-1-4200-6987-7 (Hardcover)

This book contains information obtained from authentic and highly regarded sources. Reasonable efforts have been made to publish reliable data and information, but the author and publisher cannot assume responsibility for the validity of all materials or the consequences of their use. The authors and publishers have attempted to trace the copyright holders of all material reproduced in this publication and apologize to copyright holders if permission to publish in this form has not been obtained. If any copyright material has not been acknowledged please write and let us know so we may rectify in any future reprint.

Except as permitted under U.S. Copyright Law, no part of this book may be reprinted, reproduced, transmitted, or utilized in any form by any electronic, mechanical, or other means, now known or hereafter invented, including photocopying, microfilming, and recording, or in any information storage or retrieval system, without written permission from the publishers.

For permission to photocopy or use material electronically from this work, please access [www.copyright.com](http://www.copyright.com) (<http://www.copyright.com/>) or contact the Copyright Clearance Center, Inc. (CCC), 222 Rosewood Drive, Danvers, MA 01923, 978-750-8400. CCC is a not-for-profit organization that provides licenses and registration for a variety of users. For organizations that have been granted a photocopy license by the CCC, a separate system of payment has been arranged.

**Trademark Notice:** Product or corporate names may be trademarks or registered trademarks, and are used only for identification and explanation without intent to infringe.

---

**Library of Congress Cataloging-in-Publication Data**

---

Ayers, John E.  
Digital integrated circuits : analysis and design / by John E. Ayers. -- 2nd ed.  
p. cm.  
Includes bibliographical references and index.  
ISBN-13: 978-1-4200-6987-7  
ISBN-10: 1-4200-6987-X  
1. Digital integrated circuits--Design and construction. I. Title.

TK7874.65.A94 2010  
621.3815--dc22

2009010227

---

Visit the Taylor & Francis Web site at  
<http://www.taylorandfrancis.com>

and the CRC Press Web site at  
<http://www.crcpress.com>

*To Kimberly, Jacob, Sarah, and Rachel.*

*Their patience and limitless support*

*made this project possible.*



---

# *Contents*

---

Preface.....	xv
About the Author .....	xvii
<b>1. Introduction .....</b>	<b>1</b>
1.1    Historical Perspective and Moore's Law .....	1
1.2    Electrical Properties of Digital Integrated Circuits.....	8
1.2.1    Logic Function.....	9
1.2.2    Static Voltage Transfer Characteristics .....	14
1.2.3    Transient Characteristics .....	17
1.2.4    Fan-In and Fan-Out .....	20
1.2.5    Dissipation .....	21
1.2.6    Power Delay Product.....	25
1.3    Computer-Aided Design and Verification.....	25
1.4    Fabrication.....	26
1.5    Semiconductors and Junctions.....	27
1.6    The MOS Transistor .....	28
1.7    MOS Gate Circuits .....	29
1.8    Interconnect .....	30
1.9    Dynamic CMOS .....	31
1.10    Low-Power CMOS.....	31
1.11    Bistable Circuits.....	32
1.12    Memories.....	33
1.13    Input/Output and Interface Circuits.....	33
1.14    Practical Perspective .....	34
1.15    Summary .....	34
1.16    Exercises .....	35
References .....	38
<b>2. Fabrication.....</b>	<b>39</b>
2.1    Introduction .....	39
2.2    Basic CMOS Fabrication Sequence .....	39
2.3    Advanced Processing for High-Performance CMOS.....	44
2.3.1    Copper Metal.....	45
2.3.2    Metal Gates .....	48
2.3.3    High- $\kappa$ Gate Dielectric .....	49
2.4    Lithography and Masks .....	50
2.5    Layout and Design Rules .....	53
2.5.1    Minimum Line Widths and Spacings .....	55
2.5.2    Contacts and Vias .....	57

2.6	Testing and Yield.....	57
2.7	Packaging .....	61
2.8	Burn-In and Accelerated Testing .....	63
2.9	Practical Perspective .....	63
2.10	Summary.....	63
2.11	Exercises .....	64
	References .....	64
<b>3.</b>	<b>Semiconductors and p-n Junctions .....</b>	<b>67</b>
3.1	Introduction .....	67
3.2	Crystal Structure of Silicon .....	67
3.3	Energy Bands.....	67
3.4	Carrier Concentrations.....	69
3.4.1	Intrinsic Silicon .....	70
3.4.2	n-Type Silicon .....	70
3.4.3	p-Type Silicon .....	72
3.5	Current Transport .....	72
3.6	Carrier Continuity Equations.....	75
3.7	Poisson's Equation.....	75
3.8	The p-n Junction.....	76
3.8.1	Zero Bias (Thermal Equilibrium) .....	77
3.8.1.1	Built-In Voltage $V_{bi}$ .....	79
3.8.1.2	Depletion Width $W$ .....	79
3.8.2	Depletion Capacitance .....	80
3.8.3	Forward Bias Current.....	83
3.8.3.1	Short-Base $n^+$ -p Junction .....	85
3.8.3.2	Long-Base $n^+$ -p Junction .....	87
3.8.4	Reverse Bias .....	87
3.8.5	Reverse Breakdown .....	88
3.9	Metal-Semiconductor Junctions.....	88
3.10	SPICE Models .....	90
3.11	Practical Perspective .....	91
3.12	Summary .....	91
3.13	Exercises .....	92
	References .....	93
<b>4.</b>	<b>The MOS Transistor.....</b>	<b>95</b>
4.1	Introduction .....	95
4.2	The MOS Capacitor.....	97
4.3	Threshold Voltage .....	100
4.4	MOSFET Current-Voltage Characteristics .....	105
4.4.1	Linear Operation.....	106
4.4.2	Saturation Operation .....	110
4.4.3	Subthreshold Operation.....	110
4.4.4	Transit Time .....	114

4.5	Short-Channel MOSFETs .....	115
4.5.1	The Short-Channel Effect .....	115
4.5.2	Narrow-Channel Effect.....	116
4.5.3	Drain-Induced Barrier Lowering.....	117
4.5.4	Channel Length Modulation.....	118
4.5.5	Field-Dependent Mobility and Velocity Saturation.....	119
4.5.6	Transit Time in Short-Channel MOSFETs .....	125
4.6	MOSFET Design .....	126
4.7	MOSFET Capacitances .....	133
4.7.1	Oxide Capacitances .....	134
4.7.2	p-n Junction Capacitances .....	136
4.7.3	The Miller Effect .....	140
4.8	MOSFET Constant-Field Scaling.....	141
4.9	SPICE MOSFET Models .....	142
4.9.1	MOSFET Level 1 Model .....	144
4.9.2	Berkeley Short-Channel Insulated Gate Field Effect Transistor Model .....	146
4.9.2.1	BSIM1 Parameters .....	147
4.9.2.2	BSIM1 Threshold Voltage .....	148
4.9.2.3	BSIM1 Drain Current-Linear Region.....	149
4.9.2.4	BSIM1 Drain Current-Saturation Region .....	150
4.9.2.5	BSIM1 Drain Current-Subthreshold Region .....	150
4.9.2.6	Hand Calculations Related to the BSIM1.....	150
4.10	SPICE Demonstrations .....	151
4.11	Practical Perspective .....	156
4.12	Summary .....	156
4.13	Exercises .....	158
	References .....	160
5.	<b>MOS Gate Circuits .....</b>	163
5.1	Inverter Static Characteristics .....	163
5.2	Critical Voltages.....	167
5.2.1	Output High-Voltage $V_{OH}$ .....	168
5.2.2	Output Low-Voltage $V_{OL}$ .....	168
5.2.3	Input Low-Voltage $V_{IL}$ .....	169
5.2.4	Input High-Voltage $V_{IH}$ .....	170
5.2.5	Switching Threshold (Midpoint) Voltage $V_M$ .....	171
5.2	Dissipation .....	175
5.4	Propagation Delays .....	179
5.5	Fan-Out.....	182
5.6	NOR Circuits .....	185
5.7	NAND Circuits.....	186
5.8	Exclusive OR (XOR) Circuit .....	187
5.9	General Logic Design .....	188